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Abstract
Discrete wavelet transform (DWT) is an algorithm with multi-resolution that can decompose data or signal into several components in different octave bands. In the image compression (eg. JPEG-2000 or MPEG-4), DWT can be apply on the low bit-rate compression because of its low distortion. Traditionally, DWT has been implemented by filters which require a large size of storage and complex computations. In 1996, the lifting scheme [2], a new method for constructing biorthogonal wavelet was proposed for DWT. Since the lifting scheme has several advantages, such as less hardware resource and faster computation speed. The lifting-based DWT is also used in the newest image standard - JPEG-2000.
In this paper, we propose two parts of 2-D DWT architectures. In the first part, we present an non-separable architecture for 2-dimensional lifting-based DWT. Because of downsampling of the DWT, the hardware utilization is very low. In order to solve the problem, we propose a merged and line buffer architecture, which combines the horizontal and vertical DWT together. In the second part, we add external memory and some control circuits to make the architecture suitable for different decomposition levels. Parametric design makes our circuit that can process different size of image and decomposition levels.
The proposed VLSI architectures are described in Verilog HDL, and synthesized by the Synopsys' Design Compiler. Finally, the layout of the design is generated automatically by the Avant! Apollo Layout Tools in a 0.35 1P4M CMOS technology. The Gate count number is 31093, and the clock frequency is 83MHZ.
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